



Integrated System-Level Modeling of Network-on-Chip enabled Multi-Processor Platforms

Tim Kogel, Rainer Leupers, Heinrich Meyr

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Integrated System-Level Modeling of Network-on-Chip Enabled Multi-Processor Platforms first gives a comprehensive update on recent developments in the area of SoC platforms and ESL design methodologies. The main contribution is the rigorous definition of a framework for modeling at the timing approximate level of abstraction. Subsequently this book presents a set of tools for the creation and exploration of timing approximate SoC platform models.

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